Abstract

The invention relates to a power-saving multibit delta-sigma converter (1) comprising: an input (2) for an analog input signal (ZA) and an output (3) for a digital output signal (ZD); a digital-to-analog converter (4) having a bit width N and serving to convert the digital output signal (ZD) to an analog feedback signal (Z3); a summing device (5) for solving the difference between the input signal (ZA) and the feedback signal (Z3); a filter (6) for filtering the difference signal (Z1); and a clocked quantizing device (7) for quantizing the filtered difference signal (Z2) into a digital output signal (ZD) with the bit width N. Said quantizing device (7) comprises a number of comparators (21, 22, 23) that compare the filtered signal (Z2) with a respective reference potential (U0, U6) associated with each comparator (21, 22, 23) and they each output a comparison result (V1, V2, V3) to a decoder (33), which generates the digital output signal (ZD) from the comparison results (V1, V2, V3), and the reference potentials (U0, ... U6) are updated according to a previous comparison result.